Amendments to the Specification

Please amend paragraphs [0045], [0080], [0095], [0100], [0205] and [0210] as follows:

[0045] The guide ring (5) of prior art high density plasma oxide film deposition apparatus ~~include~~ includes a first annular portion (12) and a second annular portion (10) protruding upwardly from the outer periphery of the first annular portion (12). The first annular portion (12) has a first inside diameter (16) and a first outside diameter (20), and the second annular portion (10) has a second inside diameter (18) and a second outside diameter (20) that is the same as the first outside diameter (20) of the first annular portion (12). The second inside diameter (18) is greater than the first inside diameter (16). Thus, the guide ring (5) has an inner intermediate wall extending vertically from the first annular portion (12) and which wall establishes the second inside diameter (18).

[0080] The predetermined interval (W1) between the beveled part of the semiconductor substrate (26) and the ~~upper~~ second annular portion (10) of the guide ring (5) is typically 1.75 mm. Accordingly, plasma ions migrate toward the semiconductor substrate (26) within a parasitic discharge region, namely, a region corresponding to the predetermined interval (W1), in addition to the upper surface of the semiconductor substrate (26), when the HDP oxide film deposition is performed. The plasma ions attack a beveled part (A1) of the side of the semiconductor substrate (26) at the parasitic discharge region. In particular, the attack is especially severe at a lower region (52) of the beveled part (A1).

[0095] The torn nitride film forms a break in a contact connecting semiconductor devices. Also, a loose piece of the torn nitride film can become lodged on an upper part of the semiconductor substrate during the HDP oxide deposition process, thereby causing a bridge between semiconductor device patterns.

[0100] FIG. 2A shows a semiconductor substrate having a nitride film used as a liner of a trench, according to prior art, before an HDP oxide layer is formed thereon. An active nitride film (62) and an insulating film (60) are sequentially formed on the substrate (66) over a portion of the beveled part of the semiconductor substrate (66) and over an upper surface (64) of the substrate (66), but not a lower surface (72) of the semiconductor substrate (66). In addition, the entire surface of the semiconductor substrate (66) is covered with a nitride film (70), including over the active nitride film (62) and the insulating film (60). The semiconductor substrate is processed in essentially the same manner as that shown in FIG. 1D. However, in this case, the nitride film (70) is formed to a selective thickness (T1) of 45, 50, 55 Å.

[0205] Also, the second annular portion (102) has at least three protrusions (106) extending radially inwardly toward the inner peripheral vertical side wall of the first annular portion (104). The diameter (112) of a circle inscribing the protrusions (106) is greater than that of the inside diameter (114) of the first annular portion ~~(102)~~ (104). The protrusions (106) are provided at regular intervals along the inner circumference of the second annular portion (102), whereby the angles subtended between lines connecting the protrusions (106) and the common center of the first (104) and second (102) annular portions are the same.

[0210] FIG. 3C shows the HDP oxide film deposition apparatus in a state in which a semiconductor substrate (124) has been mounted to an electrostatic chuck (108) within processing chamber (126). The electrostatic chuck (108) is disposed radially inwardly of the guide ring (100) as spaced therefrom, and is situated a little higher than the first annular portion (104) of the guide ring (100), whereby the semiconductor substrate (124) can be easily set down on the electrostatic chuck (108) and ~~pick~~ picked up from the electrostatic chuck (108). An upper electrode (120) and an electrostatic chuck (108) are connected to first and second power sources (V3, V4), respectively. The first power source (V3) preferably has a bias and a radio frequency within ranges of 2000 ~ 3000 Watts and 1.8 ~ 2.2 MHz, respectively. The second power source (V4) preferably has a bias and a radio frequency within ranges of 2000 ~ 3000 Watts and 13.37 ~ 13.64 MHz, respectively. Alternatively, the first power source (V3) preferably has a bias and a radio frequency within ranges of 2000 ~ 3000 Watts and 13.37 ~ 13.64 MHz, respectively, and the second power source (V4) preferably has a bias and a radio frequency within ranges of 2000 ~ 3000 Watts and 1.8 ~ 2.2 MHz, respectively.